

What is claimed is:

- 1 1. A method comprising:
2 scheduling processing of a packet received by a
3 packet processor with a hardware scheduler in a stack
4 processor included in the packet processor.
- 1 2. The method of claim 1 wherein the scheduling includes
2 receiving an interrupt signal from a packet engine included in
3 the packet processor.
- 1 3. The method of claim 1 wherein the scheduling includes
2 identifying an interrupt handling routine.
- 1 4. The method of claim 2 wherein a control processor in the
2 packet processor manages the packet engine.
- 1 5. The method of claim 1 wherein the scheduler uses a
2 weighted round robin scheduling scheme.
- 1 6. The method of claim 1 wherein the stack processor
2 receives the packet for a scratch ring included in the packet
3 processor.
- 1 7. The method of claim 4 wherein the stack processor passes
2 a message through a communication queue to the control
3 processor.

1 8. A computer program product, tangibly embodied in an
2 information carrier, the computer program product being
3 operable to cause a machine to:

4 schedule processing of a packet received by a packet
5 processor with a hardware scheduler in a stack processor
6 included in the packet processor.

1 9. The computer program product of claim 8 wherein
2 instructions to schedule include instructions to receive an
3 interrupt signal from a packet engine included in the packet
4 processor.

1 10. The computer program product of claim 8 wherein the
2 instructions to schedule include instructions to identify an
3 interrupt handling routine.

1 11. The computer program product of claim 9 wherein a control
2 processor in the packet processor manages the packet engine.

1 12. The computer program product of claim 8 wherein
2 instructions to schedule use a weighted round robin scheduling
3 scheme.

1 13. The computer program product of claim 8 wherein the stack
2 processor receives the packet from a scratch ring included in
3 the packet processor.

1 14. The computer program product of claim 11 wherein the
2 stack processor passes a message through a communication queue
3 to the control processor.

1 15. A scheduler comprises:

2 a process to schedule processing of a packet
3 received by a packet processor with a hardware scheduler
4 in a stack processor included in the packet processor.

1 16. The scheduler of claim 15 wherein the scheduling includes
2 receiving an interrupt signal from a packet engine included in
3 the packet processor.

1 17. The scheduler of claim 15 wherein the scheduling includes
2 identifying an interrupt handling routine.

1 18. A system comprising:

2 a packet processor capable of,
3 scheduling processing of a packet received by
4 the packet processor with a hardware scheduler in a
5 stack processor included in the packet processor.

1 19. The system of claim 18 wherein scheduling includes
2 receiving an interrupt signal from a packet engine included in
3 the packet processor.

1 20. The system of claim 18 wherein scheduling includes
2 identifying an interrupt handling routine.

1 21. A packet forwarding device comprising:
2 an input port for receiving packets;
3 an output for delivering the received packets; and
4 a packet processor capable of,
5 scheduling processing of a packet received by
6 the packet processor with a hardware scheduler in a
7 stack processor included in the packet processor.

1 22. The packet forwarding device of claim 21 wherein
2 scheduling includes receiving an interrupt signal from a
3 multithreaded packet engine included in the packet processor.

1 23. The packet forwarding device of claim 21 wherein
2 scheduling includes identifying an interrupt handling routine.

1 24. A packet processor comprising:
2 a packet engine for receiving a packet;
3 a control processor for managing the packet engine;
4 and
5 a stack processor for scheduling processing of the
6 received packet with a hardware scheduler.

1 25. The packet processor of claim 24 wherein the stack
2 processor receives an interrupt signal from the packet engine.

1 26. The packet processor of claim 24 wherein the hardware
2 scheduler identifies an interrupt handling routine.